

FCB20N60F_F085

600V N-Channel MOSFET

600V, 20A, 190mΩ

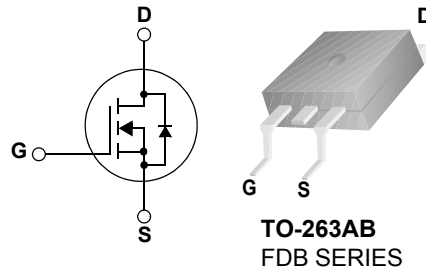
Features

- Typ $r_{DS(on)}$ = 171mΩ at $V_{GS} = 10V$, $I_D = 20A$
- Typ $Q_{g(tot)}$ = 78nC at $V_{GS} = 10V$, $I_D = 20A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging



MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rated	Units
V_{DSS}	Drain to Source Voltage		600	V
V_{GS}	Gate to Source Voltage		±30	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ\text{C}$	20	A
	Pulsed Drain Current		See Figure 4	A
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	217.8	mJ
P_D	Power Dissipation		405	W
	Derate above 25°C		2.7	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case		0.37	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(Note 3)	43	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB20N60F	FCB20N60F_F085	TO-263AB	330mm	24mm	800 units

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 10\text{mH}$, $I_{AS} = 6.6\text{A}$, $V_{DD} = 100\text{V}$ during inductor charging and $V_{DD} = 0\text{V}$ during time in avalanche
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	600	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 600\text{V}, T_J = 25^\circ\text{C}$	-	-	10	μA
		$V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}(\text{Note 4})$	-	-	500	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	4.29	5.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 20\text{A}, T_J = 25^\circ\text{C}$	-	171	195	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 150^\circ\text{C}(\text{Note 4})$	-	444	511	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	2305	-	pF
C_{oss}	Output Capacitance		-	1310	-	pF
C_{rss}	Reverse Transfer Capacitance		-	105	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	0.95	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$	-	78	102	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$				
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 300\text{V}, I_D = 20\text{A}$	-	13.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	41.5	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 300\text{V}, I_D = 20\text{A}, V_{GS} = 10\text{V}, R_{GS} = 25\Omega$	-	-	176	ns
$t_{d(on)}$	Turn-On Delay Time		-	43	-	ns
t_r	Rise Time		-	66	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	211	-	ns
t_f	Fall Time		-	42	-	ns
t_{off}	Turn-Off Time		-	-	403	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 20\text{A}, V_{GS} = 0\text{V}$	-	-	1.4	V
T_{rr}	Reverse Recovery Time	$I_F = 20\text{A}, V_{DD} = 480\text{V}$	-	163	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1285	-	nC

Notes:

4: The maximum value is specified by design at $T_J = 150^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

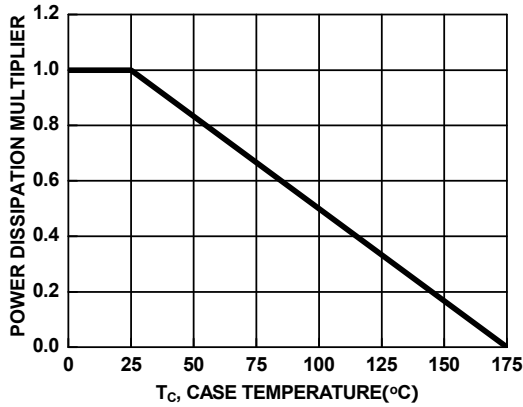


Figure 1. Normalized Power Dissipation vs Case Temperature

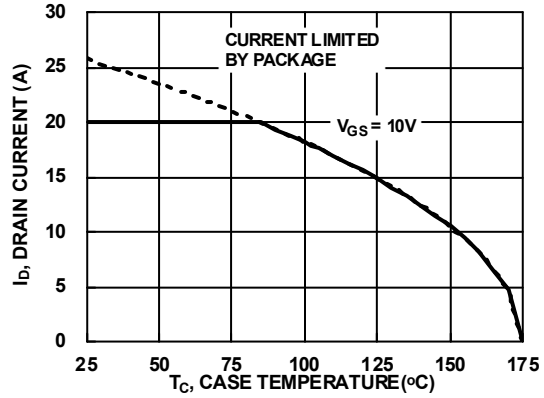


Figure 2. Maximum Continuous Drain Current vs Case Temperature

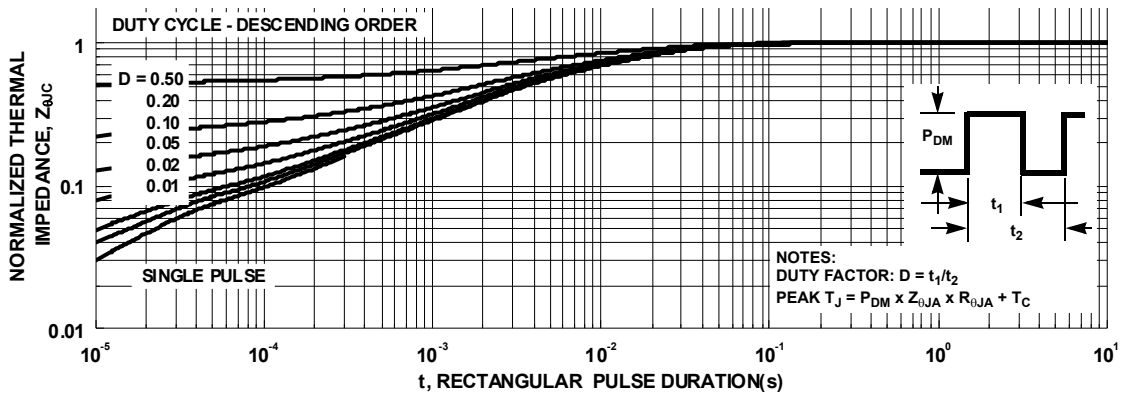


Figure 3. Normalized Maximum Transient Thermal Impedance

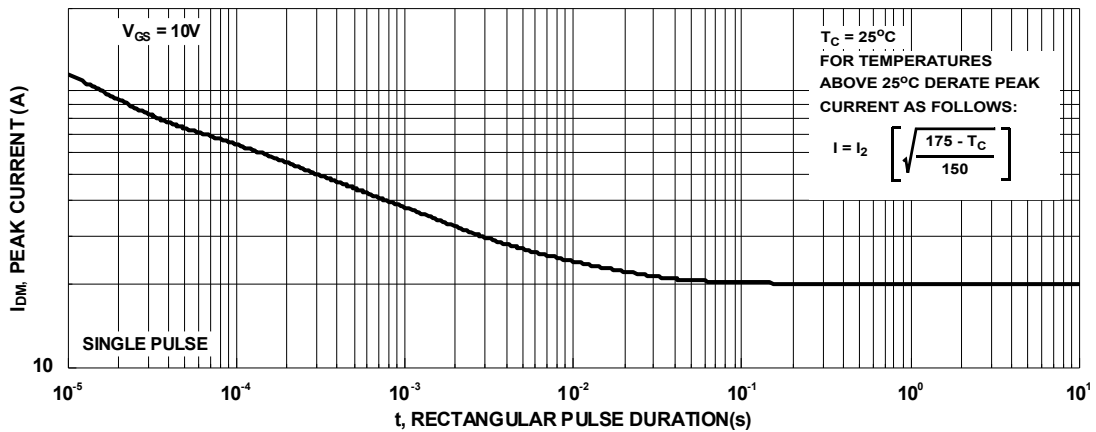


Figure 4. Peak Current Capability

Typical Characteristics

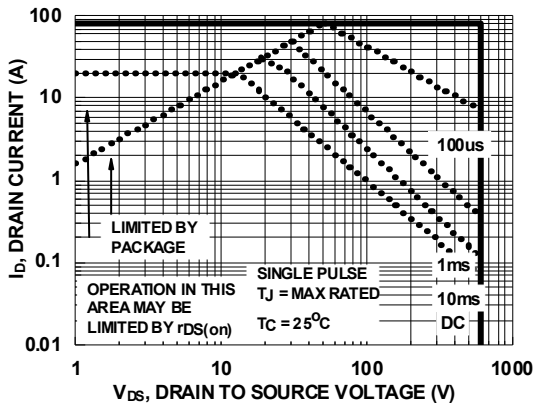
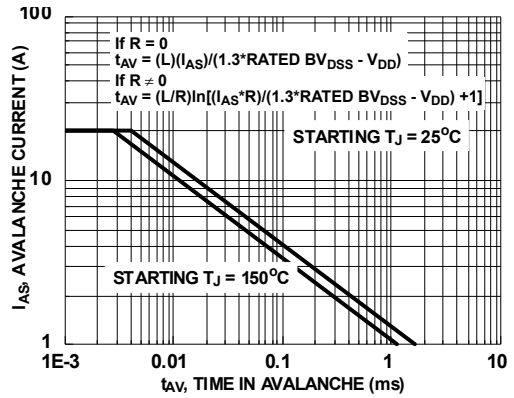


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

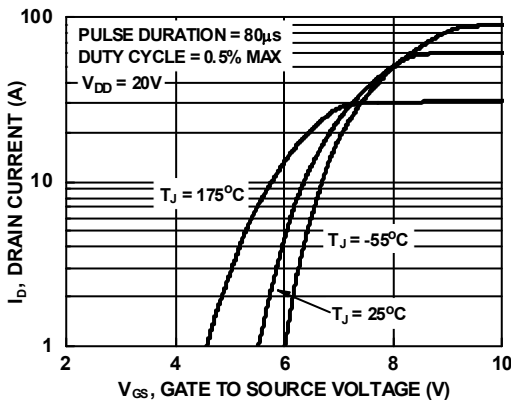


Figure 7. Transfer Characteristics

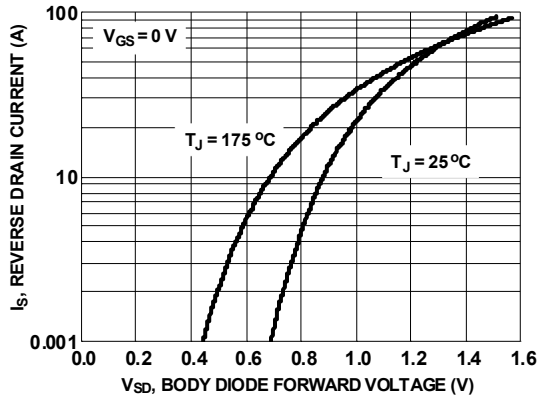


Figure 8. Forward Diode Characteristics

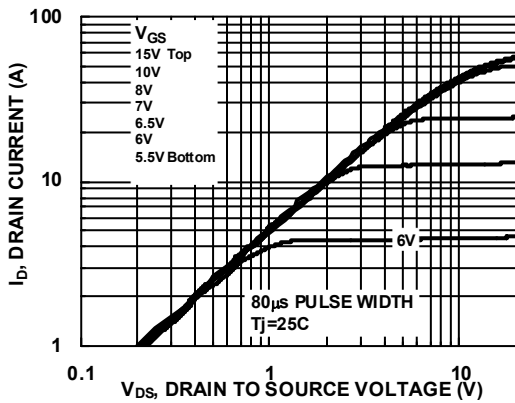


Figure 9. Saturation Characteristics

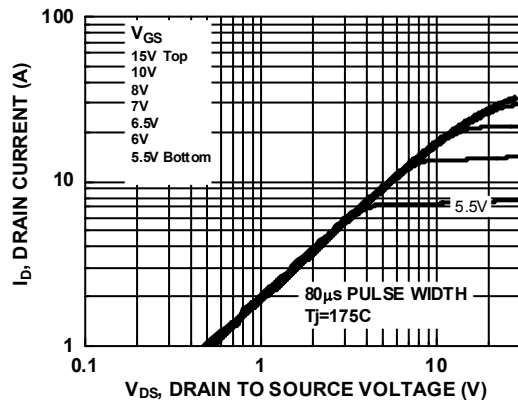


Figure 10. Saturation Characteristics

Typical Characteristics

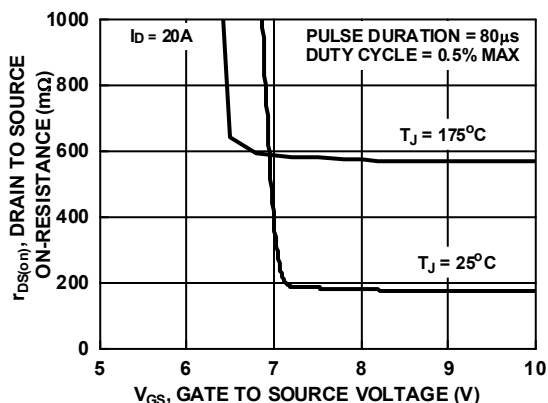


Figure 11. Rdson vs Gate Voltage

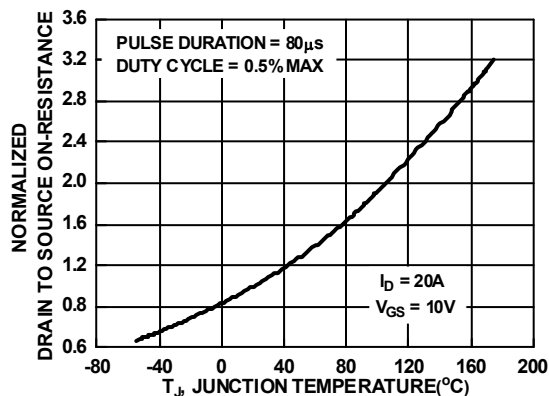


Figure 12. Normalized Rdson vs Junction Temperature

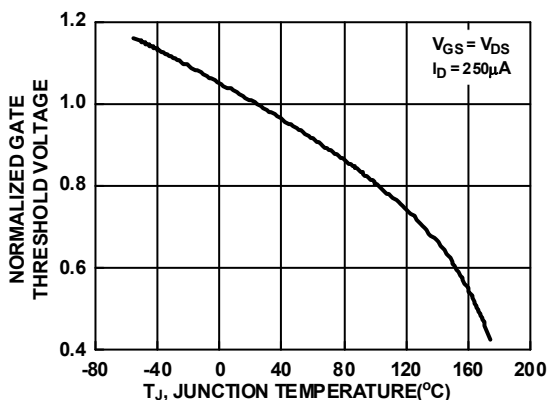


Figure 13. Normalized Gate Threshold Voltage vs Temperature

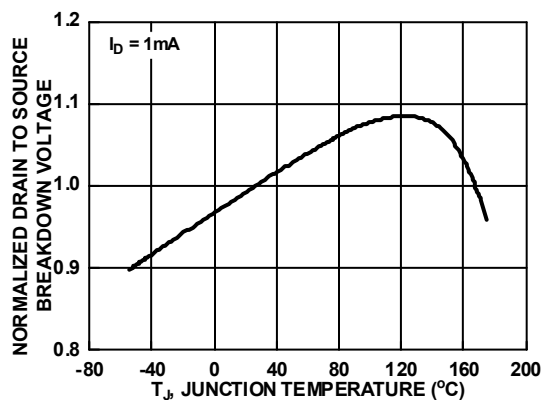


Figure 14. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

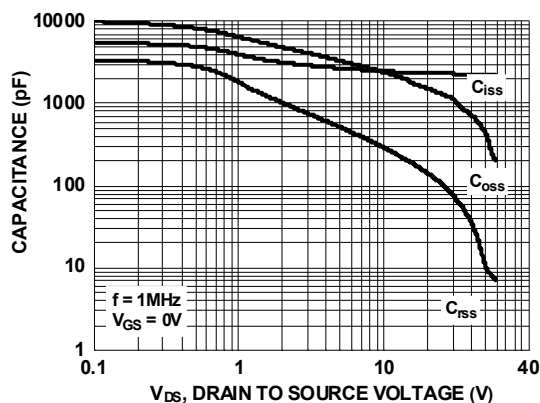


Figure 15. Capacitance vs Drain to Source Voltage

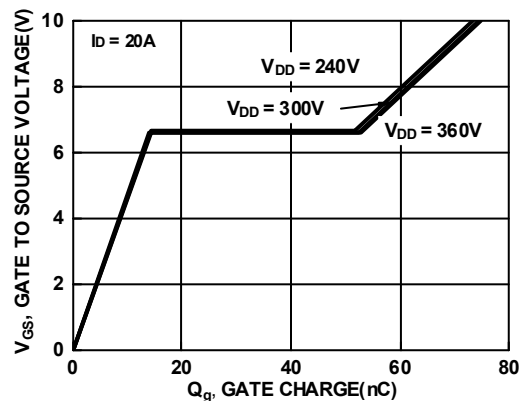


Figure 16. Gate Charge vs Gate to Source Voltage



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